being associated with state information indicating whether the copy is valid or invalid;

in each of the processors and memory that receive the request, checking to determine whether a valid copy of the block of data exists; and

returning a valid copy of the requested data from one of the other processors or memory such that only the processor or memory having the valid copy of the data block responds to the request,

as recited in claim 1.

Chang describes a system and method for maintaining translation look aside ("TLB") coherency in a data processing system. Col. 1, lines 10-13. In this system 8, in order to maintain TLB coherency, "the invalidation or other modification of a TLB entry in one processor 10 requires the invalidation of TLB entries in all other processors 10." Col. 7, lines 39-43). The TLB is a table in the processor that **contains cross-references between the virtual and real addresses** of recently referenced pages of memory, not the data itself. Thus, when a TLB entry is invalidated, it is because the data to which the TLB entry refers has been removed. According to Chang, "the entries in the TLB must be updated to reflect the presence of the new data, and the TLB entries associated with data removed from memory must be invalidated." Col. 1, lines 59-61. The **valid** designation in Chang refers to a **pointer to an address** of the data, not whether the data is invalid/valid. Thus, when a TLB entry is invalidated, a valid copy of the content of the TLB entry (i.e., the pointer to an address) is not available elsewhere. Therefore, another processor could not return a valid copy of the content of the TLB entry. Further, if the TLB entry is designated as invalid, the data to which the TLB entry points would not be available elsewhere, either, since the data would have been removed.

Chang does not discuss responding to requests for data. In particular, Chang does not disclose "returning a valid copy of the requested data from one of the other processors or memory such that ***only the processor or memory*** having ***the valid copy*** of the data block ***responds*** to the request," (emphasis added) as recited in claim 1. Instead, Chang discloses invalidating TLB entries in non-initiating processors. Further, Chang does not disclose "each

of the processors and the shared memory being responsive to a request to check itself for a valid copy of a requested block such that ***only the processor or shared memory having the valid copy responds*** to the request for the requested block," (emphasis added) as recited in claims 9 and 19.

The Examiner takes official notice of the features "***only the processor or memory*** having ***the valid copy*** of the data block ***responds*** to the request," (emphasis added) as recited in claim 1, and "***only the processor or shared memory having the valid copy responds*** to the request for the requested block," (emphasis added) as recited in claims 9 and 19. However, as discussed above, valid in Chang refers to a pointer to the address. Thus, there is no suggestion in Chang of distinguishing between valid and invalid data. Thus, it would not have been possible, as Examiner suggests, for the Chang system to include the feature of "only the processor or memory having the valid copy of the data block responds to the request," as recited, for example, in claim 1.

Further, under *In re Zurko*, 258 F.3d 1379, 59 USPQ2d 1693 (Fed. Cir. 2001), "with respect to core factual findings in a determination of patentability," conclusions may not be based on "own understandings or experience" or on an "assessment of what would be basic knowledge or common sense." *In re Zurko.* Further, "the deficiencies of the cited references cannot be remedied by . . . general conclusions about what is 'basic knowledge' or 'common sense' to one of ordinary skill in the art." *In re Zurko.* In rejecting claims 1-20, more than basic knowledge or common sense is alleged. The Examiner "must point to some concrete evidence in the record in support of these findings." *In re Zurko.* Thus, Applicant requests that Examiner point out prior art showing the features of which Official Notice was taken.

Chang does not disclose, suggest or teach "only the processor or memory having the valid copy of the data block responds to the request," as recited, for example, in claim 1. Thus, Chang does not teach or suggest the invention claimed by independent claims 1, 9 and 19. Therefore, claims 1, 9 and 19, and their dependent claims 2-7, 10-18 and 20 are allowable over Chang.

CONCLUSION

As all of the outstanding rejections have been traversed and all of the claims are believed to be in condition for allowance, the Applicant respectfully requests issuance of a Notice of Allowability. If the undersigned attorney can assist in any matters regarding examination of this application, the Examiner is encouraged to call at the number listed below.

Respectfully submitted,
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